

REMARKS

Claims 1, 2, 4-8, 10-15, 17 and 18 are pending in this application. Claims 3, 9 and 16 have been canceled without prejudice or disclaimer.

Claims 1, 2, 4-6, 13-15, 17 and 18 were rejected under 35 USC 102(b) as being anticipated by Hirata et al. (US 5,430,851, hereafter "Hirata"). The Applicant respectfully traverses, for at least the reason that Hirata does not disclose a scheduler programmed to, in a first stage, map each of at least two separate instruction groups to at least a portion of functional units independently of each other, and based at least in part on functional unit availability and instruction dependencies, perform a merging and remapping of the at least two separate instruction groups to the at least a portion of the functional units during a second stage, as recited in each of independent claims 1, 7 and 13.

The noted features clearly describe a scheduler with more advanced logic than the elements of Hirata, i.e. the instruction setup units 34 and instruction schedule unit 35 of Fig. 4, alleged by the Examiner to correspond to the claimed scheduler. More specifically, for example, nothing in the disclosure of Hirata suggests an *independent* mapping of each instruction group in a first stage, and then a *merging* and *remapping* of the instruction groups in a second stage as claimed.

The independent mapping, merging and remapping performed by the claimed scheduler is described in more detail in the present specification at, for example, page 6, lines 16-21: "Effectively, the scheduler treats each instruction group as having full access and availability to the entire processor architecture ... Subsequent merging and remapping of the instruction groups ensure that no resource conflict occurs for delivery to the functional units."

Consider, by contrast, the operations of the elements of Hirata alleged to correspond to the claimed scheduler where a resource conflict is concerned: "When a resource conflict occurs among inputted instructions in the instruction schedule unit 35, it is solved by the fixed-priority scheduling ... When a resource conflict occurs, the instruction (operational directive) inputted from the port [of instruction schedule unit 35] having smaller number is selected with priority." Clearly, these operations do not

involve a merging and remapping of instruction groups, but only deciding on one instruction in favor of another.

The Examiner cites Hirata at col. 6, lines 11-14 and col. 8, lines 48-56 as disclosing the claimed merging and remapping. However, in doing so the Examiner is linking two disparate parts of Hirata's disclosure that have no perceptible relationship to each other. Col. 6, lines 11-14 (alleged to disclose "merging") only say that "[t]he instruction schedule unit inputs decoded instructions from each of the decode units 12 to distribute them to the function execution units 16-18." This says nothing about merging instruction groups, and instead explicitly refers to *distributing* instructions. Col. 8, lines 48-56 (alleged to disclose "remapping") only say that "instruction schedule unit 15 ... may *delay* the issue of the instruction ... when there is a resource conflict" (emphasis added). But delaying is not remapping. In any event, in no way do the cited portions of Hirata, either separately or together, disclose a merging and remapping operation on instruction groups as claimed. The merging and remapping may enable optimal use of functional units as described in the present specification, for example in the paragraph bridging pages 6 and 7 and the following exemplary scenarios.

Accordingly, independent claims 1, 7 and 13 are allowable over Hirata. Moreover, the dependent claims are likewise allowable over Hirata for at least the reasons discussed in connection with the independent claims. Withdrawal of the rejection of claims 1, 2, 4-6, 13-15, 17 and 18 were rejected under 35 USC 102(b) as being anticipated by Hirata is therefore respectfully requested.

In light of the above discussion, Applicant respectfully submits that the present application is in all aspects in allowable condition, and earnestly solicits favorable reconsideration and early issuance of a Notice of Allowance.

The Examiner is invited to contact the undersigned at (202) 220-4323 to discuss any matter concerning this application. The Office is authorized to charge any fees related to this communication to Deposit Account No. 11-0600.

Respectfully submitted,

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